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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/227,174	01/07/1999	THOMAS A. PIAZZA	42390.P6702	8615

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EXAMINER
LEE, RICHARD J

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/227,174	Applicant(s) Piazza et al
	Examiner Richard Lee	Art Unit 2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 21, 2002* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *13-16, 19, 20, 22-24, and 26-28* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *13-16, 19, 20, 22-24, and 26-28* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13, 14, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eto et al of record (5,652,823) in view of Fujinami of record (5,337,086).

Eto et al discloses a video data encoder and decoder as shown in Figures 1, 2, 7, and 15, and substantially the same method and circuit for generating motion compensated video as claimed in claims 13, 14, and 26, comprising substantially the same command stream controller (i.e., 17 of Figure 7 and see column 24, lines 14-36) coupled to receive an instruction to manipulate motion compensated video data; a write address generator coupled to the command stream controller (see column 35, lines 13-30); a memory (i.e., 16 of Figure 7) coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator (see Figure 15I, column 4, and column 35, lines 13-30) and based on output from an inverse discrete cosine transform operation (see Figure 2 and column 24, lines 4-24); processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame (see Figures 2 and 7); and a read address generator (see column 35, lines 13-30) coupled to the processing circuitry and to the memory.

Eto et al does not particularly disclose, though the read address generator causing the memory to output pixel data in a second order, wherein the second order comprises reading the pixel data sub-block-by-sub-block row major order as claimed in claims 14 and 26. However, Fujinami discloses an image signal coding and decoding apparatus with multiple process motion compensation as shown in Figures 1, 3-6, and teaches the conventional breakdown of macroblocks into subblocks and the use of a read address generator for the selection of macroblock or subblock motion compensation processings (see column 4, lines 39-52, columns 7-9, Figures 1 and 6). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto et al and Fujinami references in front of him/her and the general knowledge of block processings within motion compensation video systems, would have had no difficulty in providing the read address generator for outputting pixel data in subblock by subblock major order as taught by Fujinami in place of the general read address generator of Eto et al for the same well known selective block processings as claimed.

3. Claims 15, 16, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eto and Fujinami as applied to claims 13, 14, and 26 in the above paragraph (2), and further in view of Mizobata et al of record (5,892,518).

The combination of Eto and Fujinami discloses substantially the same method and circuit for generating motion compensated video as above, but does not particularly disclose wherein the processing circuitry comprises a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and

wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed as claimed in claims 15, 16, 27, and 28. However, Mizobata et al discloses an image generating apparatus with pixel calculation circuit including texture mapping and motion compensation as shown in Figures 1, 2, 4A, 4B, 9, 10-12, 14A, 14B, 16, 17, 19A, 19B, 21, 22, 40, 41, and 43, and teaches substantially the same processing circuitry comprising a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding box are processed (see Figures 9-12, 40-43). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, and Mizobata et al references in front of him/her and the general knowledge of motion compensation and texture image processings, would have had no difficulty in providing the bounding box of macroblock data including the manipulation of pixels thereby containing all edges of a macroblock as taught by Mizobata et al for the video imaging system of Eto for the same well known purposes as claimed.

4. Claims 20, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eto and Fujinami as applied to claims 13, 14, and 26 in the above paragraph (2), and further in view of Herrera of record (6,208,350).

The combination of Eto and Fujinami discloses substantially the same method and circuit for generating motion compensated video as above, further including a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations (see Figures 2 and 7 of Eto); memory to store reference pixels (see 407, 408 of Figure 2 of Eto); mapping address generator to provide read addresses for the reference pixels (see column 35, lines 13-30 of Eto); a first in first out buffer (see Figure 8 of Eto); the read address generator coupled to a write address generator, the write address generator to generate synch points and the read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory (see column 24, lines 46-62, column 35, lines 13-30 of Eto).

The combination of Eto and Fujinami does not particularly disclose, though, the processing unit to perform texture mapping operations utilizing common circuitry; a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; the first in first out buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping filter address generator to the bilinear filter as claimed in claims 20 and 22. However, Herrera discloses a method and apparatus for processing DVD video as shown in Figures 1 and 7, and teaches the

conventional texture mapping operations and bilinear filterings within motion compensation systems (see column 14, lines 45-60). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto and Herrera references in front of him/her and the general knowledge of motion compensation video systems, would have had no difficulty in providing the texture mapping operations and bilinear filterings of Herrera within the motion compensated video system of Eto for further providing substantially the same if not the same texture mapping operations utilizing common circuitry, the bilinear filtering coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels, and the first in first out buffer coupling the mapping address generator to the bilinear filter purposes as claimed.

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eto, Herrera, and Fujinami as applied to claims 13, 14, 20, 22, 23, and 26 in the above paragraphs (2) and (4), and further in view of Tourtier et al of record (5,446,495).

The combination of Eto, Herrera, and Fujinami discloses substantially the same method, apparatus, and circuit for generating motion compensated video as above, but does not particularly disclose the apparatus is pipelined as claimed in claim 24. However, the particular motion compensation pipeline processings and multiple frame prediction operations are old and well recognized in the art, as exemplified by Tourtier et al (see Figures 5 and 7). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Herrera, Fujinami, and Tourtier et al references in front of him/her and the general knowledge of pipeline processings

within motion compensation video systems, would have had no difficulty in providing the multiple frame prediction operations in response to multiple motion compensation commands in a pipeline manner as taught by Tourtier et al as part of the motion compensation video system of Eto for the same well known purposes as claimed.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eto and Fujinami as applied to claims 13, 14, and 26 in the above paragraph (2), and further in view of Tourtier et al of record (5,446,495).

The combination of Eto and Fujinami discloses substantially the same method and circuit for generating motion compensated video as above, but does not particularly disclose the circuit is pipelined as claimed in claim 19. However, the particular motion compensation pipeline processings and multiple frame prediction operations are old and well recognized in the art, as exemplified by Tourtier et al (see Figures 5 and 7). Therefore, it would have been obvious to one of ordinary skill in the art, having the Eto, Fujinami, and Tourtier et al references in front of him/her and the general knowledge of pipeline processings within motion compensation video systems, would have had no difficulty in providing the multiple frame prediction operations in response to multiple motion compensation commands in a pipeline manner as taught by Tourtier et al as part of the motion compensation video system of Eto for the same well known purposes as claimed.

7. Regarding the applicants' arguments at pages 3-5 of the amendment filed May 21, 2002 concerning in general that "... neither Eto nor Fujinami teach or suggest a memory to store pixel

data in a first order and read out pixel data from memory in a second order where the second order is sub-block by sub-block in row major order. Thus, no combination of Eto with Fujinami teaches or suggests a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block by sub-block in row major order ...", the Examiner respectfully disagrees. The applicants' attention are directed to column 4, lines 39-52 of Fujinami for the particular teachings of wherein macroblock data are stored in frame memory 1 of Figure 1 and wherein sub-block data are being read out from the same frame memory 1. As such, it is submitted that Fujinami teaches substantially the same if not the same memory for storing pixel data in a first order (i.e., macroblock data) and to output pixel data in a second order (i.e., subblock data). Fujinami further teaches the particular selection between macroblock and subblock processings (see column 7, lines 36-58). It is therefore submitted again that it would have been obvious to provide the read address generator for outputting pixel data in subblock by subblock major order as taught by Fujinami in place of the general read address generator of Eto et al for the same well known selective block processings as claimed.

Regarding the applicants' arguments at pages 5-7 and 9 of the amendment filed May 21, 2002 concerning in general that Mizobata, Herrera, and Tourtier do not teach or suggest a memory to store pixel data a first order and read out pixel data from memory in a second order that is sub block by sub block in row major order, the Examiner wants to point out that such arguments have been addressed in the above.

Regarding the applicants' arguments at pages 7-8 of the amendment filed May 21, 2002 concerning in general that Herrera in contrast discloses a combination of a modified graphics accelerator with software to create a cost effective hybrid solution to providing a personal computer with DVD capabilities and that Herrera teaches away from Eto, the Examiner respectfully disagrees. It is submitted that both Herrera and Eto involve the particular encoding and decoding of video data, and that such texture mapping operations and bilinear filterings of Herrera may certainly be provided within the motion compensated video system of Eto for further providing substantially the same if not the same texture mapping operations utilizing common circuitry, the bilinear filtering coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels, and the first in first out buffer coupling the mapping address generator to the bilinear filter purposes as claimed.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. **Any response to this final action should be mailed to:**

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for formal communications; please mark "EXPEDITED PROCEDURE") (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Lee whose telephone number is (703) 308-6612. The Examiner can normally be reached on Monday to Friday from 8:00 a.m. to 5:30 p.m, with alternate Fridays off.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group customer service whose telephone number is (703) 306-0377.

RICHARD LEE
PRIMARY EXAMINER

Richard Lee/rl

7/31/02